Vertical Nanowall Array Covered Silicon Solar Cells

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Abstract. Highly-ordered vertical nanowall arrays were realized on Si solar cell surface to investigate their light trapping properties. High power conversion efficiency is achieved from the nanowall solar cell. In addition, nanowall array is demonstrated with great potential in the application of photovoltaic because of its stronger light trapping properties, better physical strength and maintained promise for lower material cost.

Keywords: nanostructure, nanowall, solar cell.

1. Introduction

The major motivation for photovoltaic research lies in efficiency enhancement and cost reduction. As a result, solar cells with nano-structures on the front surface has become one of the focuses for its promise to both lower the starting material’s cost [1] and maintain high efficiency. Various kinds of nano-structures such as nanowires [2], nano-cones [3], nano-domes [4] and nano-holes [5] are intensively investigated and the results demonstrate superior optical confinement effects. However, there are very few reports on another type of nano-structure, nanowalls. Unlike others, nanowall is one dimensional, rendering it interesting properties such as physical strength, interaction with light and carrier transport.

In this paper, we demonstrate our recent findings on optical and electrical properties of highly-ordered nanowall (NWall) arrays with comparative study with nanowires (NWire). Amazingly, a ~50% reduction in optical reflectance is found in NWall samples comparing to NWire. With the series resistance factored out, NWall exhibits efficiency (η) of 9.8% while the η of NWire is 9.5%.

2. Experiment
The process flow is illustrated in Fig. 1. Single-crystalline Silicon (100) p-type wafers were used. BF2/1E15cm⁻²/20keV was implanted into the backside for effective back-surface field formation. Dopant activation was done by 1000°C/5sec anneal. After cleaning, the wafers were patterned using standard lithography. Reactive ion etch was utilized for formation of well-aligned arrays of silicon vertical NWire/NWall. The NWire are with diameter of ~100nm, height of ~1.3 μm and wire-to-wire pitch of 400nm. The NWall’s width/height/pitch are 100nm/1.3μm/350nm. Subsequently, the under-surface pn junction was formed by Phosphorus implant with energy=20keV/dose=1E15 cm⁻². Finally, Ti/Cu sputter on both the backside and frontside finished the fabrication process. The metallization on wafer backside was done through shadow mask to form finger structures for effective current collection and low light blockage. The SEM image of NWire/NWall arrays is show in Fig. 2. Fig.3 is the TEM image of the NWire array. SIMS data of Phosphorus are plotted in Fig. 4.

![Figure 2. SEM image of (a) Si Nanowire array; (b) Si Nanowall array. The NWires/NWalls align orderly with each other leading to effective light trapping. The shape of the wall edge is due to diffraction effect.](image)

![Figure 3. (a) Cross-sectional TEM of Si Nanowire array showing nanowire length of 1.3 μm and nanowire diameter of 100 nm. (b) HRTEM image of Si Nanowire cross-section, showing single-crystalline lattice.](image)

### 3. Results and Discussion

Fig. 4 shows the reflectance spectrum of the samples. Integrating these data with the solar radiation power density spectrum from 300nm to 1200 nm, total reflectance of planar Si surface is calculated to be 32% of total solar power. On the other hand, NWire textured surface is able to reduce the total reflectance to 13.3% due to the interaction of nano-scaled structure with light. NWall surface further suppresses total reflectance to 6.0%, which is only half of the total solar power reflected by NWire.
Fig. 4. Reflectance spectra of Si planar surface, nanowire and Si nanowall overlapped with solar power spectrum under AM1.5 condition.

Fig. 5 shows the IV characteristics both in dark and under AM1.5 illumination for NWire and NWall textured surface devices. Comparing to a power of conversion efficiency (PCE) of 7.1% attained by our planar solar cell, a higher PCE of 8.2% is achieved for NWire solar cell. Among the three kinds of solar cells, Si planar device gives the lowest short-circuit current density (Jsc) while NWall cell outputs the highest in consistence with its strong light trapping effect. However, due to the poor fill factor of NWall devices, the overall efficiency is limited to 6.3%. This is believed to result from the relatively large series resistance (Rs) which could be attributed to the poor gap filling ability of the metal sputtering technique, since in NWall texture the requirement for the metal conformal deposition is more stringent. Therefore, NWall solar cell can readily exceed the PCE record of NWire by adopting more conformal metallization method such as electroplating.

Figure 5. I-V characteristics of solar cells under standard AM1.5 illumination for (a) planar (b) nanowire (c) nanowall solar cells
Figure 6. Multiple intensity I-V curves of solar cells for (a) planar (b) nanowire (c) nanowall solar cells

Figure 7. Forward bias dark current for (a) planar (b) nanowire (c) nanowall solar cells

Figure 8. Local ideality factor for (a) planar (b) nanowire (c) nanowall solar cells

Closer examination of the data including multiple light intensity IV characteristics [6] (Fig. 6), forward bias dark current in log scale (Fig. 7) and local diode ideality factor (Fig. 8) suggests an increasing Rs from P-Surface (1.37Ω), NWire (3.10Ω) to NWall (7.86Ω). As an estimation of the intrinsic PCE of the devices, calculation was used to eliminate the impact of Rs. As a result, high PCE of 9.5% and 9.8% was obtained from NWire and NWall devices, respectively.

4. Conclusion

We have demonstrated highly-ordered vertical nanowire/nanowall arrays on Si solar cell surface. Power conversion efficiency of 8.2% is obtained by NWire-array covered solar cell. The results indicate that nanowall array is promising candidate for both light trapping and short-distance carrier collection.
5. References


