A Non-Linear, Ionic Drift, Spice Compatible Model for Memristors

Afsaneh Shadaram\textsuperscript{1+}, Satar Mirzakuchaki\textsuperscript{2} and Farahnaz Zakerian\textsuperscript{1}

\textsuperscript{1} Islamic Azad University Science and Research Branch, Tehran, Iran
\textsuperscript{2} Iran University of Science and Technology (IUST)

Abstract. Memristor is a two terminal device which is made in nano-scale dimensions. Memristor behaves as a non-volatile resistive memory and retains the information even for a year if new voltage with different value and polarity isn’t applied to it. In this research, a simple circuit model of the memristor in non-linear ionic drift conditions has been designed for logic and memory applications. All simulations have been implemented using Hspice software. In this designed model, the obtained current-voltage curve for a sinusoidal input voltage with the amplitude of 2.1v and frequency of 1.7 MHz is hysteretic in such a way that, for writing, by applying voltage with positive and negative polarity more than threshold values (±2v), the curve will switch to low (1MΩ) and high (1GΩ) resistance, respectively. For reading, a voltage with amplitude much lower than threshold values must be applied. The changes of the memristor state (y) is shown for both sinusoidal and PWL input voltages.

Keywords: memristor, memory resistor, memristive, hysteresis, non-volatile memory.

1. Introduction

In 1971, Leon Chua represented the fourth basic circuit element named as memristor [1]. From six possible combinations of four fundamental circuit variables which are “I” (current), “v” (voltage), “q” (charge) and “φ” (flux), five of them are known. Two of these relations are given as \( q(t) = \int_{-\infty}^{t} i(\tau) \, d\tau \) and \( \phi(t) = \int_{-\infty}^{t} v(\tau) \, d\tau \).

Three other relationships are between \( v \) and \( i, \phi \) and \( i, v \) and \( q \) which define resistor, inductor and capacitor, respectively (Fig. 1).

![Fig. 1: Six possible combinations of four fundamental circuit variables.](image)

Only one relationship is undefined which is between \( q \) and \( \phi \). The element which is described by this relationship is memristor. In 1976, Chua showed that memristor poses interesting non-linear characteristics. These characteristics make memristor to be a special member of non-linear dynamic systems named memristive systems [2]. One of the interesting properties of the memristive systems is the hysteretic frequency response of Lissajous figures to sinusoidal input. After 37 years, for the first time, an HP research group, presented a physical model of memristor [3]. Consequently, some other models were presented for memristor [4,5,6].

2. The physical model of the memristor constructed in HP laboratory

The HP’s constructed memristor is in crossbar array shape made up of nanowires. At the point where two nanowires cross each other, there is a memristor. These nanowires are fabricated from Platinum and they are used as electrodes in the cross points. Between these two electrodes there is a 10 nm thin film of TiO\textsubscript{2}. This film consists of two layers. In the bottom layer the ratio of Oxygen to Titanium is 2:1, and it is an...
insulator. In contrast, in the upper layer, TiO$_2$ has lost part of its Oxygen (TiO$_{2-x}$). The Oxygen vacancies in TiO$_{2-x}$ make this layer a conductor [3]. In Fig. 2, the thickness of the thin film between two electrodes is represented by $L$. The total resistance of the device is equal to the two variable resistances connected in series. The portion of the semiconductor film that has high concentration of dopants (positive ions) has a low resistance ($R_{ON}$), and the remaining region that has a lower concentration of dopants, has a higher resistance ($R_{OFF}$). By applying a voltage $v(t)$, higher than the threshold values across the device, the charged dopants will drift. Thus, the boundary between the two regions, $w$, will move to 0 or $L$, based on the polarity of the applied voltage. By applying a voltage much lower than the threshold value, the boundary, $w$, will remain in its latest state [3].

\[
v(t) = \left( R_{ON} \frac{w(t)}{L} + R_{OFF} \left( 1 - \frac{w(t)}{L} \right) \right) i(t) \quad (1)
\]
\[
\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{L} i(t) \quad (2)
\]

where $\mu_v$ is the average of the ions mobility, $w(t)$ is the thickness of the conductor region and $i(t)$ is the current flowing through the device.

In nano-scale devices, small voltages can produce huge electric fields. These fields can cause remarkable non-linear ionic drift. In this situation, $w$ will reach L and 0 boundaries completely. The speed of movement of $w$ is almost zero in these boundaries, until the applied voltage reaches the threshold value with positive polarity. To model this condition, a window function $w(1-w)/L^2$ is multiplied by the right side of Equation (2). This makes the $w$ changes in L and zero boundaries as minor as possible [3]. But this window function will not be completely zero at L boundary. Other window functions have been proposed in order to make the changes of ‘$w$’ in both L and zero boundaries to be completely zero [4,5,7].

Fig. 3(a) indicates the applied voltage and $W(t)/L$ change as a function of time and Fig. 3(b) shows the $i$-$v$ curve for sinusoidal input in non-linear ionic drift condition[3].

\[\text{(a)}\] \[\text{(b)}\]

**Fig. 3:** (a) The applied voltage and $W(t)/L$ change as a function of time,(b) The $i$-$v$ curve for sinusoidal input in non-linear ionic drift condition.

### 3. Designed non-linear, ionic drift model of memristor using Hspice:

In this study, the designed model is based on non-linear ionic drift condition. As described before, in this situation, the switching is essentially binary. In this model, the memristor is thought of as a coupled variable-resistor shown in Fig. 4.
By replacing $y = \frac{w(t)}{L}$ in Equation (1):

$$v(t) = \left(R_{ON}y + R_{OFF}(1 - y)\right)i(t) \quad (3)$$

where $R_{ON} = 1 \text{ M}\Omega$ and $R_{OFF} = 1 \text{ G}\Omega$.

In producing $y$, the goal is to obtain $w(t) = L$ or $y = 1$ after a small delay by applying a voltage equal to or higher than positive threshold value so the total resistance becomes $R_{ON}$. Similarly, by applying a negative voltage equal to or higher than absolute value of negative threshold, $w(t) = 0$ or $y = 0$ will be obtained after a small delay so the total resistance becomes $R_{OFF}$. For voltages between threshold values, the resistance does not change and it keeps its latest value. For producing $y$, the structure shown in Fig.5 has been designed. This structure consists of a Schmitt Trigger circuit, a delay element and a switch.

![Diagram](image)

**Fig. 5:** The designed structure for producing $y$: (a) Schmitt trigger circuit, (b) Delay element, (c) Switch element.

General process design of this structure in Fig. 5 is in such a way that, whenever the memristor input voltage ($V_{in}(t)$), (which is also the input of the Schmitt Trigger), becomes $+2v$ or more, the Schmitt Trigger output, $V_{o}$, will switch to $-2v$ and then it will be delayed for a duration of $t_d$. The values used for the Schmitt Trigger circuit are:

$$
\begin{align*}
  v_1 &= v_{in}(t) \\
  \pm V_{DD} &= \pm 2v \\
  V_R &= 0 \\
  R_1 &= 1\text{K}\Omega \\
  R_2 &= 120\text{K}\Omega 
\end{align*}
$$

(4)

In memristor, switching does not occur immediately after the voltage reaches the threshold value because the ions need some time to reach the boundaries of the device. The duration of this pass through, $T_{wv}$, is calculated using the following equation [8]:

$$T_{wv} = \frac{\ln \left( 1 + \frac{L}{w(t)} \right)}{L}$$
where, \( L \) represents the length of the device, \( \mu_v \) is the average mobility of the ions and \( V_{wr} \) is the amplitude of the applied voltage for writing.

In this study, these values are selected as follows:

\[
\begin{align*}
R_{OFF} &= 1 \text{G} \Omega \\
R_{ON} &= 1 \text{M} \Omega \\
L &= 3 \text{ nm} \\
\mu_v &= 3 \times 10^{-8} \text{ m}^2/\text{s/v}
\end{align*}
\] (6)

So, by replacing these values in Equation (5), \( T_{wr} \) will be approximately 72 nsec for sinusoidal input voltage with amplitude of \( \pm 2.1 \text{ v} \) and 65 nsec for PWL input voltage with amplitude of \( \pm 2.4 \text{ v} \). To impose this delay to the memristor model, the output of the Smith Trigger, \( V_o \), will be connected to a delay element which is modeled by a dependant voltage source in Hspice and \( t_d \) is equal to \( T_{wr} \).

The delayed output, \( V_{od} \), is applied to the control input of switch and causes it to close. In this way, the voltage of node \( y \) becomes 1v and this value will be placed in the coupled variable-resistor model and the total resistance of the device becomes \( R_{ON} \). While the \( V_{in}(t) \) is lower than the threshold values, \( V_{od} \) is -2v and the total resistance remains at \( R_{ON} \). Similarly, whenever \( V_{in}(t) \) becomes -2v or less, the Schmitt Trigger output, \( V_o \), will switch to +2v and then it will be delayed for duration of \( t_d \). The delayed output, \( V_{od} \), causes the switch to turn off and the voltage of node \( y \) becomes 0v. In this way, the total resistance becomes \( R_{OFF} \). Similar to the previous case, while \( V_{in}(t) \) is lower than the threshold values, \( V_{od} \) is +2 v and the total resistance remains at \( R_{OFF} \).

4. Simulation Results

Fig. 6(a) shows the sinusoidal input \( V_{in}(t) \) with the amplitude of 2.1v and the frequency of 1.7MHz and the corresponding changes in the node \( y \) voltage. Fig. 6(b) shows the hysteretic i-v curve that is obtained from this model. This plot, similar to the hysteretic plot in the non-linear ionic drift condition (Fig.3) has binary states.

In Fig. 7, the PWL input pulse, \( V_{in}(t) \), with duration of 70 nsec and the amplitude of \( \pm 2.4v \) and the corresponding voltage change in node \( y \) is depicted. As is shown, when the amplitude of pulse becomes \( \pm 2.4 \text{ v} \), after \( t_d = 65 \text{ nsec} \), \( y \) will be “1” and it will retain this value until the pulse reaches –2.4v. Similarly, when the amplitude of pulse becomes –2.4 v, after \( t_d = 65 \text{ nsec} \), \( y \) will be “0” and it will retain this value until the pulse reaches +2.4 v. As indicated in Fig. 6 (a) and Fig. 7, the initial value of \( y \) is considered as “0”.

Fig. 6: (a) The sinusoidal input \( V_{in}(t) \) with the amplitude of 2.1v and frequency of 1.7MHz and the corresponding change in the node \( y \) voltage. (b) The hysteretic i-v curve

\[
T_{wr} \geq \frac{R_{OFF}L^2}{R_{ON} \cdot 2 \mu_v \cdot V_{wr}}
\] (5)
5. Conclusion

The operation of a memristor as a resistive memory is in such a way that its resistance depends on the amplitude, polarity and the duration of the applied voltage. In this study, a model of the memristor is designed as a coupled-variable resistor which is connected in series that operates on the basis of non-linear ionic drift. All simulations are done using Hspice software. The changes of memristor state is shown for both sinusoidal and PWL input voltages. The i-v curve of this model has binary switching in such a way that by increasing the applied voltage to the positive threshold value and more, the boundary $w$, reaches $L$ completely, and the total resistance becomes $1 \text{M}\Omega$. So, "1" will be written to the memristor. The total resistance remains in its state until the applied voltage reaches the negative threshold value. When the voltage reaches the negative threshold value and more, the boundary $w$ reaches 0, completely, and the total resistance becomes $1 \text{G}\Omega$. So, "0" will be written to the memristor and the resistance will remain in this state until the voltage reaches the positive threshold value. When the power is off, the memristor retains its latest resistance even after a year. The latter is achieved only if higher voltage with different polarity is not applied. On the basis of this property, for reading purpose, the applied voltage must be much lower than threshold values so that it does not change the state of the device.

6. References