Design of Low Power LNA for GPS Application

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Abstract. This paper presents design of Low Noise Amplifier (LNA) which operates at 1.6 GHz for Global Positioning System (GPS) application on IHP SiGe BiCMOS 0.25µm node. LNA performance is optimized for the power constraint of 2 mW. Simultaneous noise and power match is achieved. The cascode topology with resonating load is used to maximize gain at 1.6 GHz. LNA achieves gain of 14.8 dB and noise figure of 0.96 dB. The LNA exhibits IIP3 of -15.3 dBm for 2-tone test frequencies of 1.6 GHz and 1.62 GHz. The 1 dB compression point of LNA is -20.6 dBm at 1.6 GHz. Cadence tool is used for design and optimization of LNA.

Keywords: Low power LNA, SiGe BiCMOS, Heterojunction Bipolar Transistor (HBT), Global Positioning System (GPS)

1. Introduction

Global Positioning System (GPS) receivers are employed in acquisition, tracking and decoding functions. They have become standard feature of cellular and low-cost embedded applications. GPS receiver, like all other wireless receivers, invariably uses low-noise amplifier (LNA) in first few stages depending on receiver architecture. The important goals of low-noise amplifier design are low noise figure, high gain, good input-output matching and linearity. The challenge is to achieve all above at low power consumption [1]-[2].

SiGe BiCMOS technology is coming up as strong contender for high frequency applications to traditional GaAs technology. The technology employs SiGe heterojunction bipolar transistor (HBT). HBTs are bandgap engineered by graded doping of germanium in base. The device is found to exhibit excellent current gain, noise performance and linearity at modest power levels [3]. The cutoff frequency ($f_t$) and maximum oscillation frequency ($f_{max}$) of the technology used (0.25 µm) are 180 GHz and 220 GHz respectively. The fabrication of HBT is compatible with traditional CMOS process and hence lead to higher integration and lower cost. Thus HBTs are excellent choice for radio frequency application.

In this paper we present a low-power, high gain low noise cascode amplifier for L-band application. At 1.6 GHz the LNA achieves gain of 14.8 dB with noise figure of 0.96 dB, consuming only 2 mW of dc power. Section II presents the design approach and section III gives the simulation results.

2. Design of Low Noise Amplifier

The cascode topology is chosen to implement LNA. This is a combination of common-emitter (CE) and common-base (CB) configuration [4]. The transistor in CE mode acts as tranconductor while the other in CB mode acts as current buffer. One of the advantages of cascode topology is its high gain. The small signal equivalent of cascade circuit is shown in Fig. 1. Since the current gain is only due to transistor Q1 the effective transconductance ($G_m$) is given by:

$$G_m = g_{m1}$$

If $g_{m2f_{o1}}>>\beta_0$ and $\beta_0>>1$, then the output resistance is given by:
The current gain is given by:

\[ R_o = \beta o r_{o2} \]  

(2)

where \( \beta o \) is current gain. The voltage gain is given by:

\[ A_v = -G_m R_o = -g_m r_{o2} \beta o \]  

(3)

Fig. 1 Small signal equivalent of cascode

Thus the gain of cascode is \( \beta o \) times greater than that of single transistor CE stage, if we consider \( r_{o1} \approx r_{o2} \).

In this configuration input is at the base of Q1 and output is taken from collector of Q2. The cascode amplifier has higher reverse isolation. Also the miller effect of cascode configuration is very small. This enhances the stability and improves the high frequency operation of amplifier.

LNA design starts with biasing of transistors [5]-[6]. There exists a trade-off between gain and noise performance while choosing collector current density \((J_c)\). Then device size is chosen so that simultaneous power and noise matching is accomplished. For this the device is sized such that the real part of optimum impedance \((Z_{opt})\) becomes equal to source resistance \((R_s)\) i.e.

\[ \text{Re}\{Z_{opt}\} = R_s \]  

(4)

Both the steps above decide the total bias current. But in this case the total power is fixed to be 2 mW and for the given Vcc of 2 V the bias current is already fixed to be around 1 mA. So the current density and device size have to be simultaneously optimized [7]. For a fixed current when device size is increased the \( f_t \) goes down and so does the gain. \( \text{Re}\{Z_{opt}\} \) also decreases with increasing the device size. This variation is shown in Fig. 2.

![Fig. 2 Variation of \( f_t \) and \( \text{Re}\{Z_{opt}\} \) with device size. Device size is normalized with respect to m (8×[0.21×0.84µm²])](image_url)

Sometimes a compromise is made by choosing \( \text{Re}\{Z_{opt}\} \) other than \( R_s \) to obtain higher gain [7]. But here the device size is chosen such that the optimum source resistance is 50 \( \Omega \). The circuit diagram is shown in...
Fig. 3. The values of components used are given in Table I. The components $L_e$ and $L_b$ are used for narrowband input matching [2], [5]. The values are calculated as below.

$$L_e = \frac{R_f}{2\pi f_i}$$  \hspace{1cm} (5)

$$L_b = \frac{1}{\omega^2 C_{be}} - L_e$$  \hspace{1cm} (6)

But because of parasitic the miller effect the values of $L_e$ and $L_b$ are usually higher than calculated [9]. The $R_L$ used as load reduces the quality factor of resonating load thus leading to gain spread and is also used as matching element for output matching.

![LNA circuit employing cascade topology](image)

**Table 1. List of Values of Components**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_b$</td>
<td>3.1 pF</td>
</tr>
<tr>
<td>$L_b$</td>
<td>11 nH</td>
</tr>
<tr>
<td>$L_e$</td>
<td>1.8 nH</td>
</tr>
<tr>
<td>$R_b$</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>$L_L$</td>
<td>3 nH</td>
</tr>
<tr>
<td>$C_L$</td>
<td>2.3 pF</td>
</tr>
<tr>
<td>$R_L$</td>
<td>640 Ω</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>590 fF</td>
</tr>
<tr>
<td>Q1</td>
<td>120×[0.21×0.84] µm$^2$</td>
</tr>
<tr>
<td>Q2</td>
<td>120×[0.21×0.84] µm$^2$</td>
</tr>
</tbody>
</table>

3. LNA Simulation Results

The LNA designed above was simulated in Cadence tool. Various results were obtained through simulation. Fig. 4 gives the gain of LNA ($S_{21}$). We see that the gain peaks at 1.6 GHz reaching a value of 14.8 dB. The high gain is achieved due to resonating load and the spread in gain is due to the use of $R_L$ resistor.

The Fig. 5 plots input return loss ($S_{11}$), output return loss ($S_{22}$) and reverse isolation ($S_{12}$). The noise figure is plotted in Fig. 6. A very low noise figure of 0.73 dB is obtained at 1.6 GHz. High $S_{21}$ and low NF is the result of simultaneous power and input matching.

The stability of the LNA designed has also been investigated. Rollet’s stability factor ($K_f$) is given in Fig. 7. The parameter delta ($\Delta$) defined by eqn. (7) is plotted in Fig. 8. As $K_f$ is greater than unity and $\Delta$ is less than unity over the frequency range from 1.2 GHz to 2 GHz, the LNA is found to be stable over this range [1].

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$  \hspace{1cm} (7)
Fig. 4 Gain (dB) of LNA versus frequency (GHz)

Fig. 5 Input return loss ($S_{11}$), output return loss ($S_{22}$) and reverse isolation ($S_{12}$) versus frequency (GHz)

Fig. 6 Noise Figure (dB) of LNA versus frequency (GHz)

Fig. 7 Rollet’s stability factor ($K_f$) versus frequency (GHz)
4. Conclusions

A high gain, Low-noise amplifier is designed in cascode configuration using SiGe BiCMOS technology. The LNA has a dc power constraint of 2 mW. It exhibits gain of 14.8 dB, noise figure of 0.96 dB at 1.6 GHz.

5. Acknowledgements

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6. References


